WE CLAIM:

1. A method of fabricating an imaging device blooming control structure comprising:

providing a semiconductor substrate in which is configured a photogenerated electrical charge collection region;

forming a masking layer on the substrate;

providing an opening in the masking layer at a substrate location selected for a blooming drain;

forming a blooming drain by implanting an impurity into the substrate at the location of the masking layer opening; and

forming a blooming barrier region laterally adjacent to the blooming drain by implanting an impurity into the substrate at a first acute angle with the substrate to produce a lateral blooming barrier region width that corresponds to the first acute implantation angle.

2. The method of claim 1 wherein the masking layer comprises photoresist.

3. The method of claim 1 wherein the step of providing an opening in the masking layer comprises forming in the masking layer an opening having sidewalls characterized by a non-vertical profile.

4. The method of claim 1 wherein the step of forming a masking layer comprises forming at least two stacked masking layers each characterized by a distinct impurity implantation stopping power.

5. The method of claim 4 wherein the step of providing an opening in the masking layer comprises forming in each masking layer an opening having sidewalls of a distinct, non-vertical profile.

6. The method of claim 4 wherein the step of providing an opening in the masking layer comprises forming in each masking layer an opening of a distinct size.

7. The method of claim 1 wherein the semiconductor substrate is a first conductivity type and the charge collection region is of a second conductivity type, and wherein the impurity implanted into the substrate to form a blooming drain region is of the second conductivity type.

8. The method of claim 7 wherein the impurity implanted into the substrate to form a blooming barrier region is of the second conductivity type.

9. The method of claim 1 wherein the step of forming a blooming drain comprises substantially vertically implanting an impurity through the masking layer opening.

10. The method of claim 1 wherein the step of forming a blooming barrier region further comprises horizontal rotation of the acute angle impurity implantation.

11. The method of claim 1 wherein the step of forming a blooming barrier region further comprises forming a photogenerated charge barrier region at a substrate depth lower than that of the blooming drain and the blooming barrier regions by the implantation of an impurity into the substrate at the first acute angle with the substrate, a lateral width of the photogenerated charge barrier region corresponding to the first acute implantation angle.

12. The method of claim 1 further comprising forming a photogenerated charge barrier region at a substrate depth lower than that of the blooming drain and the blooming barrier region by implanting an impurity into the substrate at a second acute angle with the substrate, a lateral width of the photogenerated charge barrier region corresponding to the second acute implantation angle.

13. The method of claim 1 wherein the first acute implantation angle is selected to produce a blooming barrier region width that exhibits a short-channel effect.

14. A method of fabricating an impurity region in a semiconductor substrate comprising:

forming a masking layer on the substrate;

forming a sidewall in the masking layer at a substrate location for the impurity region,

based on masking layer impurity implantation stopping power and masking layer sidewall profile, selecting an acute impurity implantation angle with the substrate that corresponds to a prespecified three-dimensional impurity region profile in the substrate; and

implanting an impurity into the substrate at the selected acute impurity implantation angle to produce the prespecified impurity region profile in the substrate.

15. The method of claim 14 wherein the step of forming a masking layer comprises forming at least two stacked masking layers each characterized by a distinct impurity implantation stopping power.

16. The method of claim 14 wherein the step of forming a sidewall in the masking layer comprises forming in each masking layer a sidewall of a distinct, non-vertical profile.

17. The method of claim 14 wherein the step of forming a sidewall in the masking layer comprises forming in each masking layer an opening of a distinct size.

18. The method of claim 14 wherein the step of forming a sidewall comprises forming a sidewall characterized by a non-vertical profile.

19. The method of claim 14 wherein the step of forming a sidewall comprises forming an opening in the masking layer.

20. The method of claim 14 wherein the step of forming a sidewall comprises forming a masking mesa out of the masking layer.

21. The method of claim 14 wherein the step of implanting an impurity into the substrate further comprises horizontal rotation of the acute angle impurity implantation.

22. The method of claim 14 wherein the substrate is of a first conductivity type and the impurity implanted into the substrate is of a second conductivity type.